AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning at page 11, line 1 to read as follows:

FIG. 31 shows a first way of marking a package P1. Package P1 includes a chip CH1, a black layer BL, a non-black protection layer PL1 and externally applied indicia comprising a top mark TM. The black layer BL is formed on the top surface of the chip CH1. The non-black, protection layer [[PL3]] PL1 is formed on the top surface of the black layer BL. The black layer BL may be pigmented by impregnating a molding compound with carbon to make the black layer BL light absorbing. A laser-written, opaque top mark TM is formed on the exterior of the non-black, protection layer PL. There is a problem with an externally-applied indicia comprising top mark TM which is easily remarked since the laser mark TM is on the top external surface of the chip package P1. Balls B [[BL]] of a Ball Grid Array (BGA) are provided for electrical connection of circuits on the chip CH1 and mechanical connection of the chip CH1 to a connection board (not shown) is shown on the lower surface of the chip CH1.

Please amend the paragraph beginning at page 11, line 16 to read as follows:

FIG. 32 shows a type of marking in accordance with this invention for a flip-chip chip scale package P2. In this case the difference is that the package P2 comprising a chip CH2 has internal marking indicia IM formed on the top surface thereof. In this case the internal marking indicia IM are protected from damage or remarking since chip CH2 is covered, at least in part, by a non-black, protection layer PL2. The protection layer PL2 is formed directly on the top surface (back surface) of the chip CH2 and on top of the internal marking indicia IM. Note that the [[BL]] solder balls B [[BL]] are attached to the active device surface of the chip CH2.

Please amend the paragraph beginning at page 12, line 12 to read as follows:

FIG. 33 shows an alternative type of marking in accordance with this invention. In this case the difference is that the package P3 [[P2]] comprising a flip-chip (face down) CH3 has internal marking [[inidicia]] indicia IM formed on the bottom surface (that is the active device surface) thereof. In this case the internal marking [[inidicia]] indicia IM are protected from damage or remarking since chip CH3 is covered, at least in part, by a non-black, protection layer PL3 between elements of the BGA balls [[BL]] B. Protection layer PL3 is formed directly on the lower surface

(as seen in FIG. 33) of the flip-chip CH3 and on top of the internal marking indicia IM. Some chips are sensitive to light. This embodiment protects the light sensitive surface of the flip-chip CH3 from exposure to light leakage since the uncovered surface is facing the lower packaging element (not shown) which will protect the light sensitive surface of flip-chip CH3 from light.

Please amend the paragraph beginning at page 13, line 4 to read as follows:

The first step 35A is to form internal identification indicia on a surface of chip CH3 [[CH2]], in this case it is the bottom surface of flip-chip CH3, in accordance with FIG. 33. The internal marking indicia IM are preferably laser readable markings IM formed on a selected surface of the chip CH3 which in this case is the bottom surface.

Please amend the paragraph beginning at page 14, line 13 to read as follows:

A feature of the present invention is to provide encapsulation material pigmented with pigments other than opaque black pigments or to provide other light transmissive pigments and colors by providing additives which are impregnated or otherwise added to the encapsulation material.

Please amend the paragraph beginning at page 14, line 17 to read as follows:

The invention includes printing [[or]] laser marking [[and]] or forming a set of colored indicia on silicon chip front/back and forming [[use]] clear encapsulation material on the colored indicia.

Please amend the paragraph beginning at page 16, line 9 to read as follows:

FIG. 7 is a schematic cross-sectional view of a conventional Chip-Scale Package (CSP) 100 of the type manufactured by Tessera Corp. The CSP 100 has bonding pads 22 [[12]] on the bottom surface of the chip 19 that are electrically connected to respective ones of the corresponding flexible patterns 20. Insulating polyimide film 40 is bonded to the bottom surface of flexible patterns 20. The polyimide film 40 has via holes coated with a
conductive material on their inner wall, through which the flexible patterns 20 are electrically connected to solder bumps 60. An elastomer 30 is interposed between the flexible patterns 20 and the parts of the bottom surface of the chip 10 where no bonding pads are formed. The chip 19 is immobilized by a handling ring 50.

Please amend the paragraph beginning at page 18, line 18 to read as follows:

FIG. 9 is a perspective view of an attachment of a chip 210 to the TAB tape 310 with the active surface of the chips 210 attached to ~~respect-ive~~ respective pairs of corresponding polyimide tapes of the TAB 310. Then, bonding pads formed on the central part of the active surface of the chip 210 are electrically connected to respective corresponding contact leads of the TAB tape 310 via conventional bonding wires. Wire electrical connections are attached through the elongated slot of the base tapes.

Please amend the paragraph beginning at page 19, line 12 to read as follows:

FIG. 12 is a sectional view of an individual Chip Size Package (CSP) 400, taken along the line [[31-31]] 2-2 in FIG. 11. An individual CSP 400 is separated from the lead frame strip 300 by cutting the base tapes 312, that are joined to lead frame strip 300, around the area forming package body 370, using a cutting means such as a punch to produce an individual CSP 400. Each individual CSP 400 is then subjected to various reliability tests prior to shipment. In the orientation shown, the active surface of chip 210 is bonded to the lower surface of adhesive polyimide tapes 316. Bonding pads 348 formed on the central part of chip 210 are electrically connected to respective corresponding contacts 315 via wires 350. The contact leads 315 are again electrically connected respectively to corresponding via holes 318 through circuit patterns 311. The via holes 318 are electrically connected respectively to corresponding external connection terminal balls 313. Solder paste 317 may be applied on the upper surface of the base tape 312 around the via holes 318 to easily and securely mount connection terminal balls 313. The inner walls of via holes 318 are covered with a conductive coating material 318a for electrical connections. Note that the bonding pads 348 of chip 210, contact leads 315, circuit patterns 311, via holes 318 and external connection terminal balls 313 are thus electrically interconnected.

Please amend the paragraph beginning at page 22, line 19 to read as follows:

[[The]] Referring to FIG. 14, the active surface of chip 410 is attached to respective pairs of corresponding polyimide tapes 516 of the TAB tape. Then, bonding pads 448, which are formed on each side of the active surface of the chip 410, are electrically connected to respective corresponding contact leads 515 of the TAB tape via bonding wires 550. The wire electrical connections are attached through elongated slots of the base tapes 512.

Please amend the paragraph beginning at page 23, line 7 to read as follows:

FIG. 14 is a sectional view of an individual CSP 600, taken along the line 4-4 [[22-22]] in FIG. 13. The individual CSP 600 is separated from a lead frame strip 500 by cutting the base tapes 512, that are joined to lead frame strip 500, around the area forming package body 570, using a cutting means such as a punch to produce each individual CSP 600. Each individual CSP 600 is then subjected to various reliability tests prior to shipment.

Please amend the paragraph beginning at page 23, line 14 to read as follows:

A cross section of a CSP 600 according to the present invention is shown in FIG. 14. In the orientation shown, the active surface of chip 410 is bonded to the lower surface of adhesive polyimide tapes 516. Bonding pads 448_s formed on the side portions of chip 410_s are electrically connected to respective of corresponding contact leads 515 via wires 550. The contact leads 515 are again electrically connected to respective of corresponding via holes 518 through circuit patterns 511. The via holes 518 are electrically connected to respective of corresponding external connection terminals 513. Solder pastes 517 may be applied on the upper surface of the base tape 512 around the via holes 518 to easily and securely mount connection terminals 513. The inner walls of via holes 518 are covered with a conductive coating material 518a for electrical connections. Note that the bonding pads 448 of chip 410, contact leads 515, circuit patterns 511, via holes 518 and external connection terminals 513 are thus electrically interconnected.

Please amend the paragraph beginning at page 25, line 22 to read as follows:

In FIG. 22, an upper side first resin composition 12 is divided and a lower side first resin composition is under chip 5 and lead 11. A heat spreader plate [[14, 15]] of metal, such as aluminum or copper, aluminum nitride, and the like, can be placed on the encapsulant.

Please amend the paragraph beginning at page 26 , line 1 to read as follows:

In FIGS. 23 and 24, radiator plate [[15]] 14 is under upper first resin composition 12. The radiator plate 14 is preferably on the first resin composition 12, which has a thermal conductivity.

Please amend the paragraph beginning at page 26, line 4 to read as follows:

There is a possibility that a thermal expansivity, an elastic modulus, and a thickness of [[Of]] the encapsulating layer are different between the upper side of the chip (the active side) and the lower side of the chip (the bottom side).

Please amend the paragraph beginning at page 26, line 13 to read as follows:

FIG. 27 shows an example of wafer level package P with a chip C having ~~the arrangement with~~ a redistribution layer with a chip C, and ~~a BGA of~~ balls B are bonded to the face of the chip C.

Please amend the paragraph beginning at page 27, line 1 to read as follows:

FIG. 36 shows a prior art flip chip 800 marked with external markings EM. The active ~~front~~ surface 802A of chip 800 is ~~formed on~~ at the bottom thereof. Mounting pads 804 of chip 800 are connected to solder elements 806 on substrate 810 [[808]] which are connected by vias 814 to pads 812B on the base of substrate 810 [[808]]. Between the bottom ~~(front~~ surface 802A and the substrate 810 [[808] is underfill material 816. The back surface 802B of the chip 800 is on the top thereof. A cover 818 formed of black, optically opaque material, is formed over the back surface 802B and on the ~~edges and portions of the~~ sidewalls of chip 800 reaching down to be sealed with the top surface of the substrate 810 [[808]. An external mark EM is formed on the exterior surface 818A of the black cover 818.

Please amend the paragraph beginning at page 27, line 12 to read as follows:

FIG. 37 shows a flip chip 900 marked with internal markings IM, in accordance with this invention. The [[front]] active surface 902A of chip 900 is at ~~formed on~~ the bottom of chip 900. Mounting pads 904 of chip 900 are connected [[to]] through solder elements 906 [[on]] to substrate 910 [[908]] which ~~are connected by~~ has vias 914 and connected to ball grid array 912B on the base of substrate 910 [[908]]. Between the bottom ~~(front~~ surface 902A and the substrate 910 [[908]] is underfill material 916. The back surface 902B of the chip 900 is on the top thereof. An internal mark IM is formed on the back (top surface) of the chip [[800]] 900. ~~instead of the exterior surface of the cover 918 which is formed over the chip 900.~~ The cover 918 is composed of transparent material which is optically transparent is formed over the back surface 902B and on the ~~edges and portions of the~~ sidewalls of chip 900 reaching down to be sealed with the top surface of the substrate 910 [[908]].

Please amend the paragraph beginning at page 27, line 25 to read as follows:

FIG. 38 shows a wire bonded CSP P with a flexible interposer I2 to which a chip C is connected by wire bonds WB. In this case the chip C is face-up so the wire bonds WB connect to the terminals on the top surface of the chip C, i.e. the face thereof. The base of the interposer I2 carries a BGA of balls B. An internal mark IM is formed on the [[top]] back surface TP of the chip C. A cover CV composed of transparent material, which is optically transparent, is formed over the back surface [[BK]] TP and on the ~~edges and portions of the~~ sidewalls of chip C reaching down to be sealed with the top surface of the interposer I2.